REMARKS

Claim 18 has been amended to improve the readability of the claim, and not for reasons substantially related to patentability of the claimed invention. Claims 9-26 remain pending. Reconsideration of all outstanding rejections is requested in light of the following remarks. A set of replacement drawings is being submitted herewith.

Claims 9, 10, 12, 13, and 15-26 stand rejected under 35 USC 103(a) as being unpatentable over U.S. Patent Pub. No. 2003/0058345 to Morris ("Morris") in view of U.S. Patent No. 6,115,065 to Yadid-Pecht ("Yadid"). Without acknowledging that either of the cited references represent appropriate prior art to the claimed invention, Applicant submits the following remarks to overcome this rejection.

The claimed invention, as embodied by independent claims 9, 18 and 21, and as explained in more detail in Applicant's prior response dated November 23, 2004, relates to sampling pixel output signals multiple times during an integration period and storing each sampled value in a memory array located on a substrate with the pixel array. Further, independent claim 18 recites respective first and second digital memories for storing first and second sets of pixel digital values representing respective analog information output from first and second pixels.

Morris is directed to a single chip digital camera system having at least one analog-to-digital converter (ADC), register file memory, and arithmetic logic unit (ALU) associated with a block column set of pixels in a pixel array. Morris provides no teaching or suggestion relating to sampling multiple pixel output signals from the pixels during an integration period and storing each sampled value.

Yadid relates to a method and apparatus for improving the dynamic range of image sensors by achieving more than one integration time for each pixel in the image sensor for a given frame of an image. The Office Action states that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to have

Morris's imaging device sample each pixel multiple times during an integration period." Applicants respectfully disagree.

Specifically, as stated above, Morris provides no teaching or suggestion relating to multiple outputs for pixels during one integration period as in the claimed invention. Although Yadid discusses improving prior art systems by sampling multiple signals from each pixel during a frame, Yadid's teachings do not relate to a system such as that shown in Morris, having multiple register files and ALUs. In fact, Yadid teaches away from a multiple memory design, stating that it results in "reduced fill factor since two storage sites occupy considerable pixel area." Col. 3, lines 21-34. Only when applying impermissible hindsight in consideration of the teachings of the present application, would one of ordinary skill in the art be motivated to combine Morris and Yadid as suggested in the Office Action.

For at least these reasons, withdrawal of the rejection is requested. Allowance of claims 9, 10, 12, 13, and 15-26 is requested.

Further, even considering the references in combination, the references do not teach every limitation recited by claim 18 which requires first and second sets of digital values representing analog information sampled and converted for respective first and second pixels during multiple integration periods and "storing said first plurality of digital values in a first digital memory. . . and storing said second plurality of digital values in a second digital memory." Although Morris discloses more than one register file, it provides no teaching or suggesting to store a first set of signals in one digital memory array and a second set of signals in a second digital memory array, as in the claimed invention. Yadid does not cure this deficiency.

For this additional reason, reconsideration and allowance of claim 18 and claims 19-20 dependent therefrom are requested.

Further, with regard to claims 23 and 25 Applicant disagrees with the conclusion in the Office Action that "disposing the two memory arrays on opposite sides of the image sensor array" constitutes a "mere rearrangement of parts" in light of the teachings of Morris. Office Action, at 6. Specifically, Morris shows two register files 530, 550 for each block-column of pixel cells 510. The first register file 530 receives digital outputs of the ADC 520 and sends outputs to an ALU 540. The second register file 550 receives outputs from the ALU 540, which has processed the outputs from the first register file 530. This arrangement is vastly different from the claimed invention which has two memory arrays, each on a respective side of the pixel array which allows for directly receiving and storing output signals from the pixel array. This functionality is not possible in the memory arrangement taught by Morris. Therefore, it would not have been obvious to rearrange the register files of Morris as suggested by the Office Action and there is no objective motivation to alter Morris as to attain the claimed invention. For at least this additional reason, reconsideration and allowance of claims 23 and 25 are requested.

Claim 11 stands rejected under 35 USC 103(a) as being unpatentable over Morris in view Yadid and further in view of U.S. Patent No. 5,248,971 to Mandl ("Mandl"). The rejection is traversed. For whatever Mandl teaches regarding oversampling an A/D converter, Mandl does not provide the teachings or objective motivation that is necessary and lacking for combining Morris and Yadid.

Claim 14 stands rejected under 35 USC 103(a) as being unpatentable over Morris in view Yadid and further in view of U.S. Patent No. 6,466,265 to Lee ("Lee"). The rejection is traversed. For whatever Lee teaches regarding a preamplifier with adjustable gain, Lee does not provide the teachings or objection motivation that is necessary and lacking for combining Morris and Yadid.

In view of the above remarks, applicant believes the pending application is in condition for allowance. Favorable action on claims 9-26 is solicited.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Megan S. Woodworth
Registration No.: 53,655
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant